

IN THE CLAIMS

1 <sup>sub A1</sup> 1. A MOSFET logic circuit for performing a logic OR operation comprising  
 2 three transistors, wherein at least two input signals are provided to the circuit and an  
 3 output signal indicative of an OR operation performed on a first and second input signal  
 4 of the at least two input signals is output from the circuit.

1 2. The logic circuit as in claim 1, wherein the three transistors include first  
 2 and second PMOS transistors and one NMOS transistor.

1 3. The logic circuit as in claim 1, wherein first and second transistors of the  
 2 three transistors form a transmission gate outputting one signal.

1 <sup>sub A2</sup> 4. The logic circuit as in claim 1, wherein the first input signal is provided  
 2 to a source of first and second transistors of the three transistors, the second input signal  
 3 is provided to a gate of the second transistor, and a complement of the second input  
 4 signal is provided to a gate of the second transistor.

1 5. The logic circuit as in claim 3, wherein a complement of the second input is  
 2 provided to a gate of a third transistor of the three transistors.

1 6. The logic circuit as in claim 1, wherein the at least two input signals to  
 2 the circuit further comprise a complement of the second input signal.

1 *sub A* 7. The logic circuit as in claim 3, wherein when the second input signal has  
 2 *cont* a logic LOW level the output of the logic circuit is an output signal of the transmission  
 3 gate.

1 8. The logic circuit as in claim 3, wherein a third transistor of the three  
 2 transistors is a pull-up transistor, and when the second input signal has a logic HIGH  
 3 level the output of the logic circuit has a voltage level approximately equal to a drain of  
 4 the third transistor, which pulls up the output signal from the transmission gate to a logic  
 5 HIGH level.

1 9. The logic circuit as in claim 1, wherein a delay of the logic circuit is  
 2 one of a delay of a transmission gate formed by first and second transistors of the three  
 3 transistors, and a delay of a third transistor of the three transistors.

TECHNICAL